IN THE DRAWINGS:

Figures 7 and 8 have been amended to remove the reference numeral 50. This reference numeral is duplicative of the reference numeral 38, depicting the sidewalls 38 of the gate 32. Removal of reference number 50 from the drawings does add new matter to the application.

Replacement drawings are attached to this amendment.

REMARKS

This amendment is being filed in response to the Office Action dated July 19, 2005. For the following reasons, this application should be considered in condition for allowance and the case passed to issue.

The specification was objected to as not including reference sign 50 in Figure 7. It is noted that Figures 7 and 8 have been amended to remove reference numeral 50, which was a duplication of reference numeral 38, referencing the sidewalls of the gate electrode 32. The removal of reference number 50 from Figures 7 and 8, as shown in the attached replacement sheets, does not add new matter to the application. Withdrawal of the objection to the specification is therefore respectfully requested.

Claims 1-2 and 4-9 were rejected under 35 U.S.C. §102(b) as being anticipated by Gardner, et al. (hereafter "Gardner"). Claims 3 and 10-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of the remark. These rejections are hereby traversed and reconsideration and withdrawal thereof are respectfully requested. The following is a comparison of the present invention as currently claimed with the Gardner reference.

As currently claimed in the amended Claim 1, the present invention relates to a method of forming a semiconductor device, comprising the sequential steps of forming source/drain extensions in a substrate and depositing a spacer layer over the substrate and a gate electrode having a top surface and vertically extending sidewalls. A protective layer is formed on the spacer layer, and the protective layer is etched to remove the protective layer from the spacer layer over the top surface of the gate electrode and maintain the protective layer on the spacer layer parallel to the sidewalls of the gate electrode. The spacer layer is etched to remove the spacer layer from the substrate and over the top surface of the gate electrode to form spacers on the gate electrode. Each spacer has two

substantially vertical sidewalls extending parallel to the gate electrode sidewalls. A source/drain implantation is performed with the gate electrode and the spacers masking the substrate.

Similarly, in Claim 5, the currently amended claim relates to a method of forming a semiconductor device, comprising the sequential steps of forming a gate electrode having vertically extending sidewalls on a substrate and forming source/drain extensions in the substrate. First sidewall spacers are formed on the gate electrode, each first sidewall spacer having a pair of vertically extending planer sidewalls that are substantially parallel to the gate electrode sidewalls. A source/drain implantation is performed with a gate electrode in the first sidewall spacers masking the substrate. The forming of the first sidewall spacers includes: depositing a spacer layer over the substrate and the gate electrode after the forming of the source/drain extensions in the substrate; forming a protective layer on the spacer layer; and etching the protective layer and the spacer layer to form the first sidewall spacer.

In order to anticipate claims of an invention under 35 U.S.C. §102, a single prior art reference must be shown to identically disclose each and every element of the claimed invention. It is respectfully submitted that Gardner does not satisfy this high and exacting burden with respect to currently amended claims 1 and 5.

Gardner, U.S. Patent No. 6,323,519, relates to a method for making a transistor with ultrathin, nitrogen-containing MOSFET sidewall spacers using a low-temperature semiconductor fabrication process. Reviewing Figures 14-18, cited by the Examiner as disclosing the claimed invention, Gardner provides a liner 24 over a gate electrode 18. Following the formation of the liner 24, the implantation process is performed to create source/drain extensions 14, as depicted in Figure 14. This process is followed by the formation of a spacer layer 34 and implantation process to form the source/drain regions 48. It is after the source/drain implantation process is performed, as seen in

Figure 15, the spacer layer 34 and the liner layer 24 are etched, creating the spacers in Figure 16. Hence, the etched spacers are not employed in the implantation process, but rather only the unetched spacer layer and liner layer are employed during the implantation process. The amendments to the claims, particularly independent Claims 1 and 5, clarify these distinctions. Gardner performs the etching of the spacer layer and liner only after the source/drain implantation process is performed.

For example, amended Claim 1 provides a method of forming a semiconductor device, comprising the sequential steps of forming source/drain extensions in a substrate and depositing a spacer layer over the substrate and the gate electrode. Among the steps recited, the protective layer is formed on the spacer layer and is etched to remove the protective layer from the spacer layer and maintain a protective layer on the spacer layer parallel to the sidewalls of the gate electrode. The spacer layer is etched to form spacers on the gate electrode with each spacer having two substantially vertical sidewalls extending parallel to the gate electrode sidewalls. A source/drain implantation is performed with the gate electrode and the spacers masking the substrate. In other words, according to amended Claim 1, the source/drain extensions are formed in the substrate prior to the deposition and etching of the spacer layer and the protective layer. Further, the source/drain implantation is performed only after the etching of the protective layer and the spacer layer. This allows the etched spacers to be used as a mask for the substrate during the source/drain implantation. By contrast, the source/drain extensions are formed after the deposition of the liner layer 24 in Gardner. Further, the source/drain regions 48 are formed prior to any etching of the liner layer 24 and spacer layer 34. Therefore, Gardner cannot be said to identically disclose each and every element of the claimed invention as currently claimed in amended Claim 1.

Similarly, amended Claim 5 requires the sequential steps of forming a gate electrode with vertically extending sidewalls, and forming source/drain extensions in the substrate. First sidewall spacers are then formed on the gate electrode, with each first sidewall spacer having a pair of vertically extending planar sidewalls. A source/drain implantation is then performed with the gate electrode and the first sidewall spacers masking the substrate. The first sidewall spacers are formed by depositing a spacer layer over the substrate and the gate electrode after the forming of the source/drain extensions in the substrate. The protective layer is formed on the spacer layer and the protective layer and the spacer layer are etched to form the first sidewall spacer. Hence, an etching of the protective layer and the spacer layer to form first sidewall spacers is employed prior to the performing of the source/drain implantation with the gate electrode and the sidewall spacers masking the substrate. Gardner does not perform any such etching prior to the performing of the source/drain implantation. Accordingly, Gardner does not anticipate amended Claim 5 of the present invention.

For the above reasons, reconsideration and withdrawal of the rejection of Claims 1 and 5, and those claims dependent therefrom, under 35 U.S.C. §102 are respectfully requested.

The rejection of Claims 3, 10-12 under 35 U.S.C. §103(a) as being unpatentable over Gardner in view of the Remark has been obviated by the amendments made to the independent claims. The Remark does not affect the patentability of the independent claims, and therefore, since Claims 3 and 10-12 further define and limit the independent claims as amended, the rejected Claims 3 and 10-12 should now be considered allowable. Therefore, reconsideration and withdrawal of the rejection of Claims 3 and 10-12 under 35 U.S.C. §103(a) are respectfully requested.

In light of the amendments and remarks above, this application should be considered in condition for allowance and the case passed to issue. If there are any questions regarding this

amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 502624 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

John A. Hankins
Registration No. 32,029

Please recognize our Customer No. 41552 as our correspondence address.

4370 La Jolla Village Drive, Suite 700
San Diego, CA 92122
Phone: 858.535.9001 JAH:bsl
Facsimile: 858.597.1585
Date: October 7, 2005

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